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ERROR DETECTION AND CORRECTION CODE TECHNIQUES DEVELOPMENT IN MEMORY APPLICATIONS

[1] D. Pravallika, [2] N. Naga Mallikarjuna, [3]R L B R Prasad Reddy
[1]PG Scholar, Dept. Of ECE, Srinivasa Institute of Technology and Science, Kadapa – 516001.
[2]Assistant Professor, Dept. Of ECE, Srinivasa Institute of Technology and Science, Kadapa – 516001.
Associate Professor, Dept. Of ECE, Srinivasa Institute of Technology and Science, Kadapa – 516001.

Abstract

Temporary errors which are classified under soft errors are created because of fluctuations in the voltage or external radiations. These errors are very common and obvious in memories. In this paper, Diagonal Hamming based multi-bit error detection and correction technique is proposed to identify errors 1 bit error for one row, the extension for this SEC-DED-DAEC has been done to get the adjacent errors of 8 bit are correctable. By using this method, high code rate is achieved with less area and delay when in contrast to various techniques. On behalf of technology scaling, on-chip memories in a die undergoes bit errors because of single events or multiple cell upsets by the ecological factors such as cosmic radiation, alpha, neutron particles or due to maximum temperature in space, leads to data corruption. Error detection and correction techniques (ECC) recognize and rectify the corrupted data over communication channel. In this paper, an advanced error correction 2-dimensional code based on divide-symbol is proposed to weaken radiation-induced MCUs in memory for space applications. For encoding data bits, diagonal bits, parity bits and check bits were analyzed by XOR operation. To recover the data, again XOR operation was performed between the encoded bits and the recalculated encoded bits. After analyzing, verification, selection and correction process takes place. The proposed scheme was simulated and synthesized using Xilinx Vivado implemented in Verilog HDL. Compared with the well-known existing methods, this encoding-decoding process consumes low power and occupies minimum area and delay.

Keywords— Diagonal Hamming, Multibit error correction, Random bit errors and correction techniques.

I. INTRODUCTION

Two-fold data is put away in an extra room called memory. This paired information is put away inside metal-oxide semiconductor memory cells on a silicon incorporated circuit memory chip. Memory cell is a mix of semiconductors and capacitors where capacitor charging is thought of as 1 and releasing considered as 0 and this can store just a single cycle. Blunders which are impermanent or long-lasting are made in the memory cells and should be wiped out. Single piece mistake adjustment is most ordinarily utilized procedure which is fit for amending upto the slightest bit. Since innovation is expanding quickly, there are more probabilities of getting numerous blunders [1]. Utilization of Slanting Hamming strategy prompts productive revision of mistakes in the recollections. Memory was partitioned as SRAM, Measure, ROM, PROM, EPROM, EEPROM and streak memory [2]. Primary benefits of semiconductor memory is not difficult to utilize, less in cost, and have high pieces per square micrometers. Impermanent mistakes are called transient blunders which are caused due to changes in likely level. Long-lasting mistakes are caused in view of deformities during assembling cycle or huge measure of radiations [3].

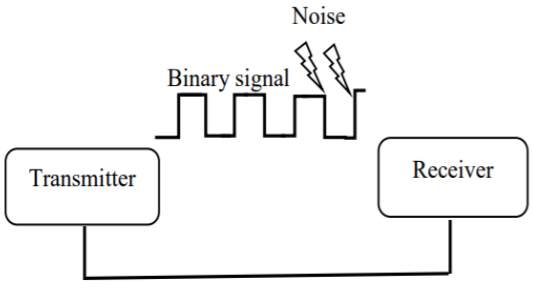

Figure - 1: Data Transmission

By and large, there are three sorts of mistakes that can be ruined in information transmission from the source to the beneficiary: • Single piece blunder: The blunder is called single piece blunder while bit changing or a mistake occurs in the slightest bit of the entire information grouping [3]. • Various piece mistakes: the happened blunders are called

different piece blunders, in the event that there are a piece changing or a mistakes in at least two than two pieces of the grouping of sent information [3].
• Burst mistakes: assuming that a blunders or pieces changing are occurred on the arrangement of pieces in the communicated codeword, then the burst mistake is happened. The burst mistake will be determined from the principal bit which is changed until the last changed piece [3]. These kinds of mistakes will be examined in section three of this report exhaustively.

II. EXISTING METHOD

a. Diagonal Hamming Code

Plan of Slanting Hamming strategy for memory Proposed plan of Corner-to-corner Hamming based multi-digit mistake discovery and revision method to the memory is displayed in Fig. 1. Utilizing this methodology of askew Hamming pieces, the blunders in the message can be perceived and can be amended which are saved in the memory. In encoding procedure message pieces are given as contribution to the Corner-to-corner Hamming encoder and the Hamming pieces are determined. Message and Hamming pieces (32+24 pieces) are saved in the memory after the encoding method.

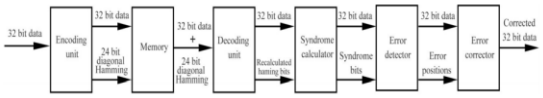

Figure – 2: Architecture of Diagonal Hamming method for Memory

III. DESIGN METHODLOGY

The proposed system used in Advanced Encryption Standard (AES), The High-level Encryption standard is a 128 cycle block figure that has been widely involved. The plan of AES was expected to be a safer substitution of DES (Information Encryption Standard).

Numerous effective equipment and programming plans have been reported, thinking about different tradeoffs of speed and region assets. The accompanying segments will give an overall practical depiction of AES with an expanded spotlight on the equipment plan of AES parts Rapid equipment Datapath's that will be pertinent in understanding the GCM Datapath will be introduced close to the furthest limit of this segment.

Each round of AES is modular and consists of four main computations namely, Byte Replacement, Blend Segments, Shift Columns, and Round Key expansion. All rounds in AES are indistinguishable except for the last round which has no Blend Sections activity. Byte Replacement comprises of 16, 8-bit word replacements while the Blend Sections activity is built from a framework multiplication. Both of these tasks are characterized by Galo is field tasks in GF (28), but there are various means to execute them. The Shift Lines activity is basically a change on the sources of info, and the Round Key activity comprises of XORing key qualities produced from a Key Timetable part. The accompanying graph represents the general round construction of AES which is rehashed in light of the key information. For a 128-bit key, a solitary round rehashes multiple times, while the 192 and 256 cycle keys have 12 and 14 rounds of calculation individually for expanded security.

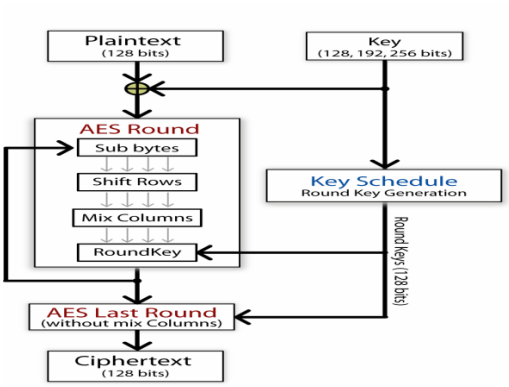

Figure – 3: Architecture of Diagonal Hamming method for Memory

An iterative plan can utilize a similar plan given above however just adds a 128bit information register toward the finish of the round structure. After a limit of 14 cycles the AES encryption result can be gotten. This iterative plan can be unrolled to make a pipelined execution that has registers set between round blocks. This is an external pipelined AES plan and a 128 digit result can be created at each clock cycle with a full pipeline. There is sufficient adaptability, nonetheless, in picking areas of the pipelined registers. Inside each of the round parts, extra pipelined stages can beaddedwith in the Sub-bytes activity which will be portrayed in

Segment 2.2.2. This is named a s an internal pipelined AES plan ,and albeit a higher inactivity and region is available, higher throughputs are conceivable. The 128 bit plain text input is planned into a state cluster which is a 4x4block of 8bit words that is controlled in each round.For the accompanying segments the state exhibit block will be utilized to portray the different round tasks so it is vital to comprehend how the information is changed into the state exhibit.

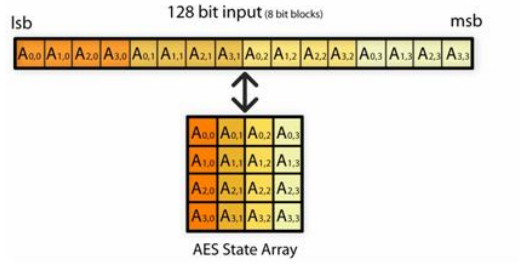

Figure - 4: AES Round State Array Transformation

A visual outline of the composite S-box. The isomorphic planning to the composite field, (GF(28) → GF((24)2)) can be carried out using a network vector duplication. The relative change comprises of a straight change followed by an interpretation which can be accomplished by a lattice vector duplication and vector expansion individually. The is amorphic planning and relative change both utilize fixed lattices that are sparse the calculation expenses of these tasks are minimal.

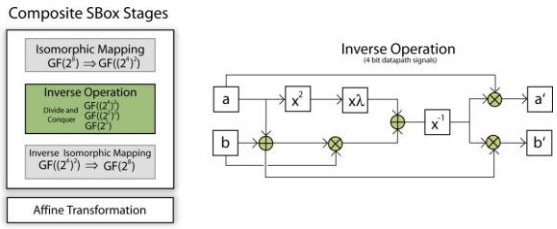

Figure - 5: AES Composite Sbox design

IV. SIMULATION RESULTS

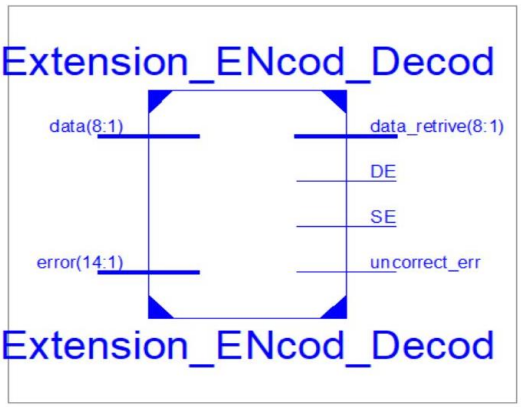

Figure - 6: Proposed Extension Encode Decode Block Diagram

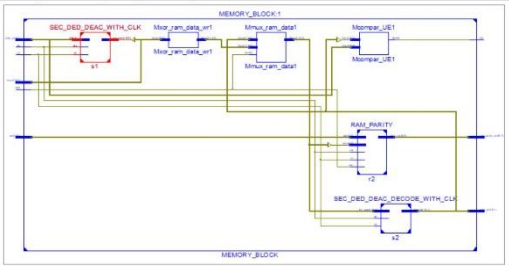

Figure - 7: Proposed memory architecture

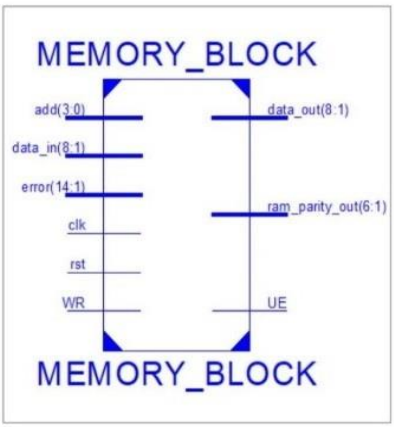

Figure - 8: Memory Block Schematic Diagram

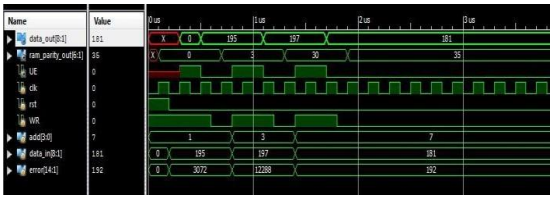

Figure - 7: Simulation Result for Memory Application

Table - 1: Difference Between Existing System Proposed System

Code Technique	Encoder input	Encoder Output	Decoder Input	Decoder output
Hamming code	1101	1100110	1100111	1100110
SEC-DED code	1100	11000011	11000000	11000010 sh=1, sp=0
			11000010	11000011 sh=0, sp=0
			11000001	11000011 sh=1,sp=1

In above figure Simulation Result the data in [8:1] and data out [8:1] are same even though there is occurrence of different error [14:1] values at different values of data and by using this memory application we can store the obtained data out values. So, the data retrieval and also data storage took place even though there is occurrence of different values of errors hence data out and data in obtained are the same values in this memory application.

CONCLUSION

As the technology scales down, various soft errors in SRAM memories were occurred due to which the single cell and multiple cell upsets were formed. Error Correction Codes such as the first technique (7,4) hamming code where 7 denotes total code word, four refers to data bits and 3 parity bits was implemented and verified its encoding and decoding processes. But it was useful only for single bit error detection and also correction which has been the main drawback of this hamming code. So, the second technique implemented was extended hamming code (8,4) or SEC-DED code ("Single Error Correction-Double Error Detection"). This code had an extra bit and used for correction of single error and also detection of double error. But correction of double error doesn't happen in SEC-DED code. So, the extension of (8,4) SEC-DED code was (14,8) SEC-DED-DAEC ("Single Error Correction-Double Error Detection- Double Adjacent Error Correction") code where 14 denotes total code word, 8 data bits, six parity bits which can be used for correction of single error, detection of double error and also correction of double adjacent error was proposed in this work.

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